ENGINEERING NOTEBOOK

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Engineering Manager of your appropriate company Division for permanent filing.

INSTRUCTIONS
1. All engineering notes, sketches, schematics, etc., are to be recorded in this book.
   Glue any inserts into the book, do not use tape.
2. Complete each sheet in its entirety, but start a new sheet on every new day that
   you wish to record information.
3. Date and sign each log sheet.
4. All log sheets containing information that might have particular significance
   must be signed and dated by one witness who reads the sheet and understands
   its contents.
   NOTE: If there are co-inventors, both should sign in the area marked WRITER,
   and a third party is required to sign as witness.
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1. Use black ink. Do not use blue ink or pencil; it is difficult to reproduce.
2. Do not try to erase. If revisions or changes are necessary, cross out and rewrite.
   See item 8 of instructions.
3. Clarity is essential but precision drawings are not required; therefore, free-hand
   sketches are acceptable.

Book No. 7652 Assigned to Joe Decuir

CONFIDENTIAL
ADJUSTING TO THIS NOTE BOOK COULD BE A PROBLEM. EVERYBODY HAS/His/Her HABITS, AND MAJOR ADJUSTMENTS ARE DIFFICULT.

ON APRIL 1, 1976 I STARTED A NOTE BOOK. RETROACTIVELY NUMBERED 13 ON 2/7/77. VERY LITTLE OF MY DESIGN WORK, OR IDEAS, PARTICULARLY FOR PROGRAMS, IS CONTAINED IN THAT BOOK.

I HABITUALLY WORK ON GREEN "ENGINEERING PADS" ANYTHING WORTH SAVING WINDS UP IN BINDERS.

I SUSPECT THAT THE DOMINANT VALUE OF THIS BOOK IS LEGAL DOCUMENTATION OF FREQUENT IDEAS. MY GREEN SHEETS SERVE FINE FOR GETTING THE WORK DONE, BUT I DOUBT THAT THEY WILL STAND UP IN COURT.

ANOTHER FUNCTION OF THIS BOOK MAY BE SO THAT AN "ENGINEERING MANAGER" CAN EVALUATE MY WORK. THIS IDEAS CONSTITUTE A PROBLEM, SINCE THE LINES OF AUTHORITY HERE ARE NOT CLEAR. I DO WHAT NEEDS TO BE DONE, WITH PRIORITY DETERMINED BY CONSSENSUS WITH JAY MINER, LARRY WAGNER, AND BOB BROWN, AND NILES STROHL, THE STELLA PROJECT ENGINEER WITHIN THE CONSUMER PRODUCT ENGINEER GROUP DOWN THE HALL.

IF ALL ELECTRONICS FABRICANTS IN TO A CHIP DEVELOPMENT GROUP AND A SOFTWARE DEVELOPMENT GROUP, MY ROLE WILL BECOME CONFUSED.

THOSE ARE MY THOUGHTS ON WHAT SHOULD GO IN HERE; AND IF ANYONE DESIRES BOB BROWN THINKS HE HAS ANYTHING TO ERIE POINT IT, HE/She SHOULD SPEAK SOON. I SEE REGARD DR. BROWN AS MY BOSS.

[Signature] AFTER MY BICYCLE, A STELLA SY-73
WHAT SHOULD GO IN THIS BOOK:

**DAILY SUMMARY**S & IDEAS ABOUT:

- NEW SYSTEM ARCHITECTURES, INCLUDING CHIPS.
- DEVELOPMENT SYSTEM ARCHITECTURES.
- FUNCTIONAL SPECIFICATIONS FOR SOFTWARE:
  - CHIP DIAGNOSTICS
  - BOARD DIAGNOSTICS
  - DEVELOPMENT SYSTEM DIAGNOSTICS
- GAME (APPLICATIONS) SOFTWARE.
- SOME INTERNAL SPECIFICATIONS FOR ABOVE SOFTWARE.
- THOUGHTS AND OBSERVATIONS ABOUT OTHER SYSTEMS, CHIPS SETS (EX: SIGNETICS)
- IDEAS FOR GAMES FROM COIN &

**DAILY SUMMARIES & PROBLEMS ENCOUNTERED IN DEVELOPMENT SYSTEM WORK.**

MAYBE OTHER THINGS WHEN I THINK OF THEM.
PADDLE GAME CODE.

TO DATE A 4 PLAYER - 2 PADDLE/PLAYER SOCCER
GAME HAS BEEN WRITTEN FOR STELLA.
I AND STEPHEN RANECKE ARE CONSIDERING IT
TO A 4 PLAYFIELD/16-32 PADDLE CONFIGURATION
SYSTEM OF VERTICAL PADDLE GAMES. THIS GAME
SET WILL BE SUBMITTED TO THE GROUP
FOR PLAY-TESTING OUT AND COMMENTS.
IT WILL USE BOTH OPTION AND GAME SELECT.
AFTER COMMENTS IT WILL BE BOILED
DOWN INTO A SPECIFIC GAME SET, USING
GAME SELECT ONLY.

THAT A SET OF PADDLE GAMES INCORPORATING
HORIZONTAL PADDLES, INCLUDING BASKETBALL, FOOTBALL,
AND VOLLEYBALL (REBOUND) WILL BE PURSUED.
(I WOULD HOPE THAT MR. RANECKE GETS TO DO THIS).
I WILL THEN PURSUE BREAKOUT, PIN PONG
(1/6 SCALE), AND A WHEELS GAME FOR
SEARS.

AFTER THAT, I DON'T KNOW.
I WILL BE TRAINING NEW PEOPLE
AS PROGRAMMERS AND FOR HARDWARE SUPPORT.
I WILL HELP JAY, STEVE WAYER, AND HARRY
WAGNER TO ARCHITECT A POSITION TO STELLA.

CONFIDENTIAL
GAME OR PROJECT
STELLA

DESIGN OF PADDLE GAME SYSTEM.

TIMEOUT

VSYNC START
EXAMINE CONSOLE

PLAY
CHECK Ball
GAME SELECT
CLEAR SCREEN

VBLANK START

CHECK FOR BALL SCORE
SEIZE IF SCORE TIMEDOUT.

BORDER BALL OFF PF
BORDER BALL OFF PRODG.

SET UP PADDLE CONFIGURATION ACCORDING TO OPTION NUMBER
SET UP PADDLE ACCORDING TO GAME NUMBER
SET UP COLOR/LUM REGISTORS ACCORDING TO COLOR/WIII SWITCH AND GAME NUMBER

SET UP PADDLE ACCORDING TO POT POTS.

DISPLAY GAME AND OPTION NUMBERS

DISPLAY SCREEN
(WITH OR WITHOUT BALL)
3RD, 4TH FEBRUARY - WROTE AND DBUGGED ATARI MUSE CODE.
INSTALLED GAME NUMBER DEPENDANT PLAYFIELD AND COLORS. & W SWITCH SOFTWARE.

MONDAY & TUESDAY 7TH & 8TH FEBRUARY
MOST TIME SPENT FIRE FIGHTING.

NILES STROHL DESIGNED AND INSTALLED A MODIFICATION TO KIM DEVELOPMENT SYSTEM THAT MIXES SOUND IN WITH VIDEO INTO TO SPEAKER. IT WORKS SATISFACTORY, W/O SERIOUSLY DEGRADING LOW FREQUENCY RESPONSE OF AUDIO.

SOME KINDS OF SPURIOUS PROBLEMS ARE OCCURING BETWEEN THE BOARD AND LARRY WAGNER'S PROGRAMS. SOME FAULTS TRACED TO KIM SYSTEM RAMS, BUT THERE ARE INDEPENDANT.

WEDNESDAY, THURSDAY, FRIDAY, 9, 10, 11 FEB.
NUTS & BOLTS STUFF.
GETTING STELLA READY FOR MARKET TESTING.

MONDAY 14 FEB. MORE OF SOME.
NOTES ON DESIGNING A GI TANK AND OTHER CHIPS IN THE GI BOOK

OBJECT RESOLUTION LOOKS CONSERVED FROM THE SPECS. "8/160" OR SCREEN VS. 8/160 FOR SPECTRUM.

MOTION SOUNDS FlIPPER, "32 ROTATIONS" "32 DIRECTIONS"
US 16 ROTATIONS AND DIRECTIONS FOR SPECTRUM.

3 FORWARD AND 3 REVERSE SPEEDS
REVERSE SOUNDS USEFUL - BUT I DON'T KNOW ABOUT MULTIPLE SPEEDS.
THESE ARE EASY TO DO WITH THE TIME FEATURE.

THEY HAVE MINES, AND THEY HAVE BULLET EXPLOSIONS.

SCORING - 1 IN GI - GAME RESTARTS AT 81.
USE - GAME ENDS AT 10
- WE COULD INC. UPPER LIMITS OF SCORER, BUT IT MIGHT JUST INCREASE LENGTH OF GAME

WE DON'T HAVE A GENERAL PURPOSE MICROPROGRAMMABLE CHIP, TO GENERATE SINGLE CHIP GAMES.
NOS TECHNOLOGY'S GAME CHIP, AND ARCADE ARE BOTH EXAMPLES OF SUCH A DEVICE. WE COULDN'T CONSIDER SUCH A MACHINE FOR A 1978 PRODUCT.
For example,

Why not look at the
MOS Technology 65C02/April 79
6532 Trio.

Design a special-purpose machine that executes a micro code
(perhaps in an expository ROM) which is (at a flow chart level) similar to
that executed by similar programs.
- Except that there are fewer variables
- And more special-purpose instructions.

EX:
RIGHT NOW THE 65C02 DISRUPTS THE
TANK GRAPHICS LINE PAIR BY LINE PAIR

Suppose a micro programming machine
has a register for object x vertical
position, and a register for object x
display, and an n x n bit pattern
for object x graphics.

A single instruction might
do a comparison of VPOS and LINE COUNT
and decode range, and Installing graphics.
A second instruction would branch on RANGE.
A third instruction would lead disc into
graphics.

Play field could be a register ROM.
THE BASIC IDEA I SUPPOSE IS TO GO FOR THE MIDDLE GROUND BY BUILDING SINGLE CUSTOM (+ MINOR STD RAM/ROM) WHICH CAN DO SMILE (40) SET OF GAMES - TAKE SOME SYSTEM FUNCTIONS AND REPLICATE INTO ARCADE LIKE SYSTEMS.

BALL / PADDLE INTERACTION ALGORITHMS.

1) SIMPLE. \( |HM| = 1 \).
   \[ \text{SIGN}(HM) = \text{function of player } \# \]  \[
   VM = \text{function of impact point } -2 \rightarrow 2 \]

2) \( |HM| = 1, 2, 3 \)
   \[ \# \text{HITS} = 0, 1, 2, 3 \rightarrow 1 \]
   \[ \# \text{HITS} = 4, 5, 6, 7 \rightarrow 2 \]
   \[ \# \text{HITS} \geq 8 \rightarrow 3 \]
   \[ \text{SIGN} = \text{function of player } \# \]
   \[ VM = \text{function of impact point} \]

3) \( |HM|, VM = \text{function of impact point.} \)

\[
\begin{array}{c}
(1, +2) \\
(2, +1) \\
(3, 4) \\
(2, -1) \\
(1, -2)
\end{array}
\]

\[
\begin{array}{c}
1 \\
2 \\
1 \\
2 \\
1
\end{array}
\]

\[
\begin{array}{c}
1 \\
2 \\
1 \\
2 \\
1
\end{array}
\]
4) "ENGLISH"

\[(V_{m+1}, H_m) = \Phi (V_{m}, H_m, \text{impact point})\]

\[
\begin{align*}
V_m &= V_m + 1 & |H_m| &= |H_m| - 1 \\
H_m &= V_m & |H_m| &= |H_m| \\
V_m &= V_m - 1 & |H_m| &= |H_m| + 1
\end{align*}
\]

\[
H_m = 1, 2, 3, -1, -2, -3 \quad V_m =
\]

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>(H_m)</td>
<td>(\Phi (\text{impact pt}))</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(-2 \leq V_m \leq +2)</td>
</tr>
<tr>
<td>2)</td>
<td>(\Phi (# \text{of hits}))</td>
<td>(\Phi (\text{impact pt}))</td>
</tr>
<tr>
<td></td>
<td>(-3 \leq H_m \leq +3, # \geq 4)</td>
<td>(-2 \leq V_m \leq +2)</td>
</tr>
<tr>
<td>3)</td>
<td>(\Phi (\text{impact pt}))</td>
<td>(\Phi (\text{impact pt}))</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(-2 \leq V_m \leq +2)</td>
</tr>
<tr>
<td>4)</td>
<td>(\Phi (\text{impact pt, } H_m))</td>
<td>(\Phi (\text{impact pt, } V_m))</td>
</tr>
</tbody>
</table>

\[\text{Audio volume} = |H_m| \times 4.\]

\[\delta_2 = |H_m| + |V_m| \times 2\]

\[\delta_2 = \Phi \text{ function of impact point.}\]
IF 11 PINS ARE USED ON A SSI/MSI MUX TO CONTROL A DYNAMIC RAM ARRAY, IT HAS 13 LEFT IN A 28 PIN PACKAGE, AND 24 LEFT IN A 40 PIN.

AS A MINIMUM, A DEDICATED ADDRESSING SHAPE, IT NEEDS:

2 +5, GND
2 OSC IN, 2 IN
8 D0 - D7
9-10 2-3 CHIP SELECTIONS

R/W
3-6 ADDRESS LINES
21-22 LINES
1-4 VIDEO OUT (1 IF PIPED INTO SPEAKER, 4 IF CHASSIS LUMINANCE)
22-26 RAM CONTROL
33-37 RAM CONTROL

=> 40 PINS

IF THIS IS A STAND ALONE SYSTEM:

DELETE A CHIP SELECT.
ADD A COLOR DELAY INPUT.
ADD A D0 OUTPUT
ADD A DQ OR RDY OUTPUT
ADD 4 IN 2 OUT AND 4 OUTPUTS.
ADD 4 BULK OUTPUTS

4-5
33-37
41-42
GAME OR PROJECT

NEW MACHINES

ADD A CHARACTER CHIP TO TIA

IT COULD FIT INTO THE SAME

MEMORY SPACE AS THE TIA:

19 WRITE ADDRESSES FROM (2D TO 2F) \[ \frac{3F}{2C} \]

\[ \frac{13}{13} = 19 \]

READ ADDRESSES

OR USE ONE CHIP SELECT ON A/B6 TO DISTINGUISH IT FROM STRA - GIVING IT 64 R/W ADDRESSES.

COULD USE THE RDY LINE IN PARALLEL WITH TIA FOR RESYNCHRONIZATION - OR HAVE MICRO DO THAT ITSELF W/TIA.

COULD ENCODE ITS OUTPUT INTO TIA ON ONE OR TWO LINES, OR MIX THEM EXTERNALLY BY WIRING OR ON CHROMA AND LUM LINES.

2 +5, GND
2 G, OSC
8 D9 - D7
8 2 CHIP SELECTS AND 6 ADDRESS LINES AND NO R/W
10 3 CHIP SELECTS, AND 3 ADDR — 6 ADDRESS LINES AND R/W
28 - 30 + VIDEO OUTPUTS
1 - 4 120° INTO TIA OR 3-7 VIDEO OUTPUTS
28 - 34 TOTAL PINS,

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GAME OR PROJECT

NEW MACHINES.

Suppose use 4 write addresses only.

\[ A1, A0 = \]

\[ \begin{array}{c|c}
0 & 1 \\
1 & X \\
2 & X \\
3 & X \\
\end{array} \]

Control Word
Shift register data - write 20 times.
Writable character address
Writable character data.

Put in locations 40 - 7F redundantly.

\[ CS0 = A1Z \]
\[ CS1 = A7 \]
\[ CS2 = A6 \]
\[ A1 = A1 \]
\[ A0 = A0 \]

5 lines CS/AD.

2 power
2 clocks
8 data
17 pins
7 pins for output.
24 pin package.

By 1 line into TIA - COLO
or 1 line into TIA for turn on
2 CUM, 1 CHR, 1 CH DR.
3 IDEAS:
1) 3 LEVEL SCREEN MAPPING
2) DISPLAYING NUMBERS, CHARACTERS
3) SCANNING A KEYBOARD.

1) 3 LEVEL SCREEN MAP IS NECESSARY FOR BOARD GAMES, DOMINOS, POKER, CHECKERS, AND OTHERS.

SPEIFICALLY IDEA IS TO WRITE ACHIEVE IMAGES ON ALTERNATE FRAMES.
SO THAT THE TOTAL SCREEN IS WRITTEN FURN 2 FRAMES.

3 LEVELS — PF. WRITTEN ODD FRAMES
2 — BACKGROUND
2 — PF. WRITTEN EVEN FRAMES

(1A) LARRY KAPLAN'S IDEA: TWO LEVEL SCREEN MAP.

1) TURN OFF PROJECT.
2) WRITE RIGHT SIDE OF PLAYFIELD ON ONE FRAME, WITH COLPO = 0, COLPI = 3040200000
3) 2ND FRAME, WRITE LEFT SIDE, COLPI = 23, COLO n = 3040200000
CARE SHOULD BE TAKEN IN THE MIXING OF COLORS. 
PF COLORS AND BACKGROUND COLOR.
2A) **Displaying Numbers, Characters.**

- Six characters to 60 pixels (as in a word) = 3/10 of screen.
- P0, P1, P2, P3 same column.
- Line pairs.

\[ \text{Mus1} = 3 \]
\[ \text{Mus2} = 3 \]

42 bytes of image, written out real fast.

4 bytes / line

- (5x7) dot matrix characters.
- 6 to 8 (depending on space between characters)

---

IF YOU USE LARRY KAPLAN'S IDEA.

- PD P1 P3 P1 P5 P1 PD P1 P3 P1 PD P1 P3

Do the same thing, except write the left six bytes on one frame, and the right six bytes the next frame.

3A) **Display Numbers, As 5x3 Matrices.**

- As in score mode now.

**Future using Playfield now:**

- 8 digits.
- 10 digits.
GAME OR PROJECT
FEASIBILITY IDEAS

3d) OR USE PLASTIC TO DISPLAY NUMBERS

12 small digits.

OR 2 LARGER PAIRS × 1 PLAYER, x4

All this is good for displaying smaller numbers here and there, or even for implementing a calculator!?
4) KEYPAD.

THE CONTROLLERS HAVE A LOT OF WIRES.

1 8-BIT BIDIRECTIONAL PORT (NOT TRUSTED)
2 VIA INPUT PORTS - HIGH IMPEDANCE (PULLUPS INSIDE)
4 POT PORTS - (SLOW)
14 LINES

SEVERAL MATRICES:

9) 2x8 = 16

[Diagram of a 2x8 matrix switch with labels and connections]
4d) $4 \times 6 = 24$

$\text{PA5}$

$\text{PA6}$

4c) $7 \times 8 = 56$ Kbits(!)
5) Some day, somebody ought to do MiNYA: GUILFIGHT.

8 x 12
GRAPHICS.

USE PLATFORM AS FIXED OBSTACLES.

6, 7, 8) STAPLECHASE
SPACERACE
DOMINOS
FLYBALL
ETC.

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BACK TO PADDLE GAMES:

HOCKEY
SOCCER
PONG (TENNIS)
HANDBALL
BASKETBALL
VOLLEYBALL
QUADROPOLE

DIFFERENT PADDLE CONFIGURATIONS.

ADD GRAVITY TO
HANDBALL?

DECEM
15/12/79

WITNESS

DATE
GAME OR PROJECT
SPRINT - 16 KEY HEADER.

16 KEYS.

\[ 5V \times 0.68 \mu F = \frac{5V \times 17 \mu F}{A} = \frac{0.55 \text{ms}}{64 \mu \text{sec/line}} \]

To get two more keys, use the following connections:

Scan each input at the end of a frame before checking the status.
C) OR EXPAND IT. \( 16 \times 3 = 48 \) KEYS.

D) OR EXPAND IT DIFFERENTLY. \( 8 \times 4 = 32 \) KEYS.
Remember to write down my FTC Program Solution.

In ATARI mode, for STELLA games, generate slow Vsync and use it to toggle all color and luminance bits to each pixel, so that all places on screen values get all possible luminance and chroma values, randomly distributed, so that the TV does't get burned in.

- Characterize color delay line

<table>
<thead>
<tr>
<th>$V_{DC}$</th>
<th>$V_{OC}$</th>
<th>Burst Duty Cycle</th>
<th>Green (End) Duty Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.02</td>
<td>5.02</td>
<td>25/55: 48.2%</td>
<td>20/55: 36%</td>
</tr>
<tr>
<td>5.65</td>
<td>3.02</td>
<td>Green Delay</td>
<td>230 nsec</td>
</tr>
<tr>
<td>4.51</td>
<td></td>
<td></td>
<td>280 nsec</td>
</tr>
</tbody>
</table>

- Characterize equivalent Trubel1 unit points:

<table>
<thead>
<tr>
<th>$V_{EC}$</th>
<th>4.6V</th>
<th>5.03</th>
<th>5.4V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising Threshold</td>
<td>1.90</td>
<td>2.02</td>
<td>7.05</td>
</tr>
<tr>
<td>Falling Threshold</td>
<td>1.42</td>
<td>1.45</td>
<td>1.45</td>
</tr>
</tbody>
</table>
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GAME OR PROJECT
STELLA - 6532 PORTS - CHARACTERIZATION.

6532

PWR

Difficulty Switch

VR

0.53 mA
0.005

IR

0.021

VR

0.21K

R

0.52K

876 mA

1.05K

VR

1.61K

VR

2.24K

VR

3.15K

VR

3.64K

VR

5.32K

VR

Virtually no hysteresis observed in 6532 port.

VR

6532 reads "1"

VR

6532 reads "0"
Stella - Changes to Chip.
STELLA - CHARACTERIZE PORT PULLDOWN.

\[ R \quad V_I \quad I_{mA} \quad V_{BLANK} \]

<table>
<thead>
<tr>
<th>R (K)</th>
<th>V_I</th>
<th>I (mA)</th>
<th>( \Omega ) equiv.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.71</td>
<td>.305</td>
<td>.995</td>
<td>3.06</td>
</tr>
<tr>
<td>3.87</td>
<td>.357</td>
<td>1.197</td>
<td>2.98</td>
</tr>
<tr>
<td>3.28</td>
<td>.407</td>
<td>1.397</td>
<td>2.91</td>
</tr>
<tr>
<td>2.67</td>
<td>.487</td>
<td>1.686</td>
<td>2.90</td>
</tr>
<tr>
<td>2.16</td>
<td>.588</td>
<td>2.038</td>
<td>2.89</td>
</tr>
<tr>
<td>1.78</td>
<td>.698</td>
<td>2.411</td>
<td>2.89</td>
</tr>
<tr>
<td>1.48</td>
<td>.824</td>
<td>2.815</td>
<td>2.72</td>
</tr>
<tr>
<td>1.18</td>
<td>1.010</td>
<td>3.373</td>
<td>2.99</td>
</tr>
<tr>
<td>.99</td>
<td>1.192</td>
<td>3.836</td>
<td>3.11</td>
</tr>
</tbody>
</table>

CONFIDENTIAL
Problem: How to do fast 5-bit ADC with single supply available on a controller input.

One way: Successive approximation in analog:

Sample and hold.

All amplifiers are same National LM324's.

This is analog successive approximation (asynchronous).

Might need sampling, w/ DAC amp and CMOS switch.
CONSIDER MOTOROLA MC14549B
MC14559B

START COUNT
FROM MPU

S/6 HYF SCHMIDT.
(74CO4)

MAYBE BUFFER ANALOG INPUT.

CONFIDENTIAL
GAME OR PROJECT
SHELLA

1 2 3 4 5
DE-93.5
0 0 0 0 0
0 0 0
0 0

14.APR.77

1 2 3 4 5 6 7 8 9
FORWARD, PA 4,1
BACK, PA 5,1
LEFT, PA 6,2
RIGHT, PA 7,3
PO T 0,2
TRIGGER, 14.15
VCC
62ND
PO T 1,3

CONFIDENTIAL
ENGINEERING LOG SHEET

GAME OR PROJECT

OCCURRING

SAID

VIDEO

MUSIC

GENERIC

CHARACTER

SPACES

TWO

WILL

SELL

LOT

CHARACTERS

BAD

PERSON

GOOD

DESIGN

SAMPLES

PREPARED

COMMERCIAL

CHIP

DIES

PRODUCT

WRITER
DATE
WITNESS
DATE
GOOD FINAL IDEA
VIC
PARTS TO COMPLETE WORK TENT
OCT 32
16 BIT
VIC WIRESPECT TO 2600

6800 - $10 AREA

FEBRUARY, MARCH, PARTS
APRIL, MAY, PRODUCTION

CPU SAVE + INSTRUCTIONS
TO RUN 160 + 60 XT,

DECREMENT MODULUS INSTRUCTION!!!

REGISTRER INDIRECT ACCESS MODE
AUTO DECREMENT 8/16 BIT TIMING

TRIAGE TO OPTIMIZE THIS TO RUN VIC,

2K/16K ACBBY (COMMON DECIDE!)

EXTERNAL MEMORY

13 BIT IC

WRITER: L. Freind DATE: 1/2/77 WITNESS DATE: 
6800 - Could be a drill.

With 40 lines, outbox print等功能可实现。

NEEDED FILE

 Trên list of requirements:

6509 "more @ a company"

VIC requires 200 more disk access.

<table>
<thead>
<tr>
<th>SYSTEM</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIC DES</td>
<td>6520 (?</td>
</tr>
</tbody>
</table>

VIC DES

MONO ACCESS

2 RAMS MESSRS

2 NTSC PAL or SECAM.

BIG AUDIO SYNTHESIZER

SAYED'S END SYSTEMS

C/T FIX BALANCE S/TIVI

$45 for chip set
CLOCK ON OR OFF

CLOCK AND COIL

DIFFERENT MODEL BOARD VS. H.39101

CONFIDENTIAL
HOST IDEA: USE MODULATED TV MIA

METHOD FOR TRANSMITTING VIDEO TO

ÒORDINARY TV WITH MODULATING MODULATOR

ADVANCED: IF NO ELECTRICAL CONNECTOR

FROM GAME TO TV.

Perhaps game/computer does not have to real

TYPE I APPROVAL.
14 JULY. MOS TECHNOLOGY,
RAY HIRT.
WILL WATHAMS

CHIP SIZE ESTIMATES ON
SEVERAL APPROACHES.
DELIVERY DATES FOR SAMPLE & PRODUCTION.

1) (6507 + PARTS OF 32)
2) (6507 + 6510 KITTINER) + 6810.
3) (6507) + (REDUCED 32)
4) (6507) + (REDUCED 32 UV & RAM) + 6810.

US 5) 6507 + 6532 AS IS.
6) *5) - I/O TEST

PARTS OF 32 WE USE:
- PA, BIDIRECTIONAL
- PB, BID INPUT
- TIMER: 1, 1/8, 1/64
CAN BOUNCE IN $\phi_2$ (1.2mHz)

IF YOU DON'T BOUNCE OUT
ADDRESS MULTIPLEXED WITH DATA

CAN BE BONDED (LAIID OUT)
WITH $\phi_2$

CS
AS
AΦ
FOR STELLA

CAN BE BONDED.

$\phi_2$

CS
AΦ

AΦ $+$
TAKES 1 DAY TO PREP WORK
TO LAY OUT PRINTER.

MASK TURNAROUND IN 1 DAY - 1 WEEK

6-8 WEEKS FOR REASONABLE
TURNAROUND.

TURNAROUND FOR DIFFERENT MASK
IS THE SAME AS ANY
PERIPHERAL CHANGES.

SAMPLES IN FEBRUARY.

EMULATE IT
WITH 6522'S AND
6502, AND RAM AND ROM.

APPROXIMATE: 32K x 8, 512K x 8
64K x 8, 1K x 8
128K x 8, 2K x 8
VIC

Horizontal: 258 Clocks
192 Dots
Example

Turn off display by
dothing it off screen.
No interrupts from VIC -
  turn off screen software.

Can runs e 14/3.5/4.

16 bytes of control

0.1 Horizontal and vertical position of
top left of display w/ respect
  to HSYNC

HSYNC \div 81 from
does

2.3 V.H. Line size counter

Composite w/ composite sync, composite line,
composite color.
ADDRESS COMPUTATION.

12-BIT LATCH

12-BIT LOAD
MEMORY
SCAN
COUNTER

COUNT UP,
JAM LOAD
COUNT UP
JAM LOAD

COUNT UP, AND RELOAD LATCH
JAM LOAD
COUNT UP

(No H or V reflect)
2 POTS - 8 Horizontal Lines per Conversion 8 Bits.

U8 CHIPS 4052B FOR EXPANSION.

26 A, B, C, D, E SOUND.

12 BIT WORD MEMORY FOR COLOR.

QUADRATURE GENERATOR on CHIP.

COLOR - Sin + Cos - 2

DIFF AMP on CHIP.

8 COUNS

WHITE, BLACK + SIX COLORS

TWO COLORS CHROMA.

TWO COLORS LUM.

AUDIO - SINE GENERATOR (7 BIT WAVE) + 1 16 BIT POLYNOMIAL CRT.
GAME OR PROJECT
ADDA

MPU 6502
PIA 6520
512K 8K RAM
2K 8K ROM
VIC RF

32 COLOR / 14 LINES

Perhaps change VIC
To run at slower clock-
Turn off processor
To allow double
Frequency & characters.
GAME OR PROJECT
KAY - 12 KEY KEYBOARD

6532 PINS CAN
SOURCE .53 mv into
Φ VOLTS - (see p25
this notebook) - look
like 10K resistors
pullups.

if all switches are closed
one PA port has to sink
6 other pullups. $\Delta V/\Delta I = 3mA$
⇒ it will choose.

if pullup R on ID and II
= 10K - it takes

non simultaneous
⇒ single keys
by writing a single
Φ AND B "GOES ON PORT A"
and, after sufficient
charging time, reading
ID, II, and I4 for "Φ"s

IF TWO KEYS ARE DEPRESSED
SIMULTANEOUSLY, IGNORE
ALL OF THEM. DESELECT A
KEY WHEN A SINGLE
KEY GOES UP

00 ⇒ 11101110 EE
01 : 11011110 DD
10 : 10111011 BB
11 : 01110111 77
CHOICE OF PULLUP RESISTOR

Pulling up:

\[ RC \ln 0.6 = 0.440 \mu s \]

If \( R = 10\, \text{k}\),

\[ C = 236 \mu s \quad @ \quad 5\, \text{k} \]

\[ C = 177 \mu s \quad @ \quad 3.3\, \text{k} \]

Pulling down:

\[ R_{C} = 1.8K + \frac{250}{250 + R} \]

\[ 1.328 \, \text{C} \quad @ \quad R = 5\, \text{k} \]

5V

3V

1.5V

5 \times \frac{250}{250 + R}
250 \parallel 10K = 54.4 \Omega \\
250 \parallel 5K = 238 \Omega \\
250 \parallel 3.3K = 284 \Omega \\

R = 2K \times 68\text{nf} = 136\mu\text{sec.} = t \\

\times \times \times \times 
if \ R = 5K \quad \frac{250}{5.45K} \times 5.00 \quad 5.00 \\
\quad \frac{5.45K}{5.00} \times 5.00 \quad = 0.238 \text{ volts.} \\
\quad 181\mu\text{sec.} = 1.328 \times 136\mu\text{sec.}
GAME OR PROJECT
PAL STELLA

EXPERIMENT

1) DISCONNECT AUDIO IN MODULATOR NETWORK FOR OLD KIM SYSTEM (MOUNTED ON BOARD)

2) TUNER MODULATOR FOR 62.25 MHz

3) CONNECT RF OUT TO GAME TV-SET TO CHANNEL 3.

4) ADD VERTICAL LINES TO VERTICAL BLANK AREA IN COMBAT GAME CODE.
   314 LINES OF 68 FRAME.

DERIVATION:

\[
\frac{3579575 \div 2}{228} = \frac{313.99517 \text{ LINES/FRAME}}{50}
\]

LOOKS OK!!

TANK ASPECT RATIO OK.
GAME OR PROJECT
PAL STELLA

\[ 4.43361875 \text{ Hz} \times \frac{4}{5} = 3.5468949 \text{ Hz} \]

\[ \frac{325}{15.6113} = 15.556.556 \text{ kHz} \]

Error in MHz

\[ \frac{15.556.556 \text{ Hz}}{50 \text{ Hz}} = 311.13113 \text{ lines/frame} \]

612 vs 675

\[ \frac{3.5795454 \text{ MHz}}{3.5468949 \text{ MHz}} = 1.009205 \]

1.182 MHz to CPU.

\[ \text{DEC.} \]

\[ 4.4336 \]

\[ \text{PAL CHRO.} \]

\[ \text{4T5 TRAN NTSC COVER} \]

TIA A/B

\[ \text{CO4} \]

\[ \text{CO1} \]

\[ \text{CO2} \]

\[ \text{CO3} \]

\[ \text{VOL} \]

\[ \text{BUST WINDOW} \]

Adjust

CONFIDENTIAL

DERAL LOG SHEET

DATE: [redacted]

WITNESS [redacted]
GAME OR PROJECT

WORMSNAKE 6509

FRANK MAHONY - STER

STEP SIMON - SYSTEM DESIGN

TED BAINES - SYSTEM DESIGN

BIL NORD - PROGRAMMING

OVERVIEW:

3 temp ranges
3 speed ranges
will FP3
new variances
new memory support
new memory
new interface
1,2 chip mini systems (6801, 6802+6544)
high performance upgrade of 6500

MPS up for renewal in Oct '77

CONFIDENTIAL

Source tape compatible - but not object compatible

95% 95% 95% - commit spec at end 8 6 '77

INTRODUCE 3RD QTR '78
On chip clock. 5V, bus compatible

8 bit word size 16 bit access

2MHz minimum clock

Target 200m Hz

No illegal decode

Memory RDY,
Instruction SINC
Bus Request BUS Grant

Perhaps

Fast IRQ (Just PC and Status) limit the clocks

Please add at least one Accumulator

IRQ acknowledge - useful select

IRQ may be vectored by driver

"2MHz" required 225 nsec accesses

Increase size of address drivers

Keep data, address, OZ, R/W

+4

A15

A0-A15

D0-D7

CONFIDENTIAL
TWO ACCUMULATORS
TWO INDEX REGISTERS
TWO STACK POINTERS - 1 as in
PHEM2 bus architecture
DIRECT PAGE POINTER
14 BIT WIDE
not doing low bit-high style
chip designer wanted to do it
not source compatible
upperword source compatible.
80 Instruction consistent memories.
348 or cases
8 x 8 multiply
unsigned AxB -> A,B
mostly for index calculation.
16 bit operations
bit manipulation in memory
powerful stack instructions
register transfer exchanges.

ADDRESSING MODES
11 ADDRESSING MODES

7 bit of
offset
±16

DIRECT VIA PAGE POINTER
INDIRECT ADDRESSING ADDED TO INDEXED MODES.
UP TO 14 BIT DIXED INDEXED OFFSET.
ADD INCREMENT DECREMENT
ACCUMULATION INSTRUCTION. A+=X
A,B + 2 BYTES IN MEMORY.

FIF COMPUTATIONS ON INX, DEY -> create odd immediate to index register.
SOFTWARE DESCRIPTION

- POSITION INDEPENDENT CODE
- NON SELF-MODIFYING CODE
- STRUCTURED, HIGHLY DOCUMENTED CODE
- MULTITHREADING AND MULTITASKING
- STACK OPCODE Compiler Instructions
- OPERATING SYSTEM CALLS: 3 DIFFERENT
  - 2 BIT CALLS
  - 1 16 BIT CALL

RCS, IRC, FIRE, HAI, SAI.
OSC 1, OSC 2, OSC 3.

8 BIT

<table>
<thead>
<tr>
<th>DIRECT PAGE PTR</th>
<th>COND. CODE REG.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>IX</td>
</tr>
<tr>
<td></td>
<td>IY</td>
</tr>
<tr>
<td></td>
<td>US</td>
</tr>
<tr>
<td></td>
<td>SP</td>
</tr>
<tr>
<td></td>
<td>PC</td>
</tr>
</tbody>
</table>

DECODING & BRANCH ISN'T BRANCH INSTRUCTION.

LOAD MACRO INSTRUCTION

ACCESSING MODE: LIMITED
DIRECT
IMMEDIATE
INDEXED (ABS)
INDIRECT AUTOINC
INDIRECT DECR INC
INDIRECT DECR DEC
IMMEDIATE INDEXED
IMMEDIATE DIRECT
HDL INDEXED
HDL DIRECT

TOTAL INSTRUCTION: 15
OPTIMAL INSTRUCTIONS

- Position, Incremented LoC
- Next, Self-Monitoring Code
- Structured, Hardly Subprogrammed Code
- Multitasking and Multiprocessing
- Stack Directed Complex Instructions
- Operating System Calls
  - 3 Different 5 2 Bit Calls
  - 1 10 Bit Call

RES, I & FIRE, NMI, SWI
OSC 1, OSC 2, OSC 3.

8-bit

<table>
<thead>
<tr>
<th>DIRECT PASS PTR</th>
<th>LOAD CODE REG</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>IX</td>
</tr>
<tr>
<td></td>
<td>IY</td>
</tr>
<tr>
<td></td>
<td>US</td>
</tr>
<tr>
<td></td>
<td>SP</td>
</tr>
<tr>
<td></td>
<td>PC</td>
</tr>
</tbody>
</table>

Decoding & Branch Next Branch Instruction.

LOAD MEMORY IMMEDIATE

Addressing Mode

DATA:

- DIRECT
- INDIRECT (ABS)
- INDIRECT INDEXED (X)
- INDIRECT INDEXED (Y)

ALSO LOAD constant

WITNESS
There exists a double length carry decrement and branch word and 8 bit length.

16 bit instructions:

- Double ADD
- Load STORE
- COMP
- SUBTRACT
- DECIMAL/INCREMENTS/NEG
- USE GROUP NOT EQUAL
- SIGN EXTENT, SET MEMORY

Bit manipulation:

- BIT SET - OR 0/Memory
- BIT CLEAR - AND 0
- BIT TEST
- TEST 1 SET
- BIT CLEAR - XOR 0/Memory.

Relative inst.

- LOAD PROGRAM RELATIVE
- LONG BRANCH TO SUBROUTINES
- LONG BRANCH 8
There exists a double length memory requirement and structure for 16-bit and 2-bit

BIT INSTRUCTIONS:

DOUBLE

LOAD
STORE
CLEAR
SUBTRACT
DECIMAL, DECIMAL, HEX
AND CARRY NOT EQUAL
SUCH EXTENTS SET没想到

BIT MANIPULATION

BIT CLEAR - 02 01/11/77
BIT TEST - 01 02/11/77
TEST 4 SET
BIT CLEAR - 02 01/11/77.

OTHER INSTR.

LOAD PREVIOUS RELATIVE
LONG BRANCH TO SUBROUTINES
LONG BRANCH #
SUBROUTINES & INTERRUPTS:
- RETURN USING RETI
- RETURN FROM FAST IRQ
- STOP = CALL IF STK
- Operating system calls (3)
- Software resolution of IRQ, FIRQ, NMI
  (still have want for interrupt)

SOFTWARE RESET
Should reset whole system.

REGISTERS
- Transfer register to register
- Exchange and register
- ADD TO R, Y, U, N, S immediate
- ADD TO R, Y, U, N, S
- LOAD, STORE, ST, XOR, AND, CONDITION coding
- LOAD STORE A, B, X, Y, U, S, CCR, D, DP
- LOAD LAMBDA Y, U, N, S, AND D

INSTRUCTION:
- BNE = B IC
- DEC A, INCREA, NOT Incre
- DEC A, ADD A, W, B
- Instruction, subtract A from B
- ADD A, EQUAL TO accumulate

[Signature]

DATE: 12
WITNESS: 
DATE: 
A 16K based simulation to plug into TASER.
"2 25K's + microcode"
TEST CIRCUIT FOR JAY'S
LOCKED OSCILLATOR: 1054°

OSCILLATORS:

\[ \text{4.433 MHz} \]

\[ \text{3.539 MHz} \]

CONFIDENTIAL
They will develop 2 new models of 8000 series, which will be specific to particular market segments.

Get our opinions on things that are useful for us.

They are 2nd sourced with

review of 8800 architecture.

Look into CPU details.

I/O is cruel of memory mapped.

Addressing modes

WORKSPACE REGISTER
DIRECT REGISTER
INDIRECT WITH AUTO INCREMENT
INDEX: Immediate register
SYMBOLIC (DIRECT)
TRAP/JMP
PC RELATIVE (JUMP)
ALL

PROGRAM CONCEPT

LOGICAL

SHIFTS & BIT SHIFTS

I/O (CRT CONTROL)

RETURN

3 MHz clock 500 ns memory,

BRANCHE 2.67

ADD 4.67 R-L

MIPY 17 µsec. 16 x 16

DIV 41 µsec. 16 x 16

MUL 7.83 REG TRANSFER
SEP 940  19  1980

TMS 9930  MULTIPLEX DATA BUS
14 LOCATION CLOCKS
ON CHIP CLOCK!!

TMS 9940  SAMPLE 1ST TIME

128 BYTES RAM
2K ROM IN CHIP & EPROM
4 INTERRUPT IN
16 BITS OF CPU.

32 GENERAL I/O LINES

25% BITS EXTERNAL.

POWER DOWN MODE
STOPPED OPERATION
CLOCK OSCILLATOR ON CHIP
14 BIT AT 1MHZ.

PIPELINED 8-BIT MACHINE INTEGRAL.

8 KOPS — SOFTWARE INTERRUPT.

MULTIPROCESSORS INTRODUCED
— SERIAL PORT FROM TO
ANOTHER DEVICE, BIT RATE
1200 BPS, 9600 BPS, 7.5 KHZ.

SEPARATE POWER FOR RAM, FLAGS, REGISTERS
AND FOR EVERYTHING ELSE.
. est. (240 mil)²  est. $10 price  "design goal"

Poor memory expansion.

Kevin McDonough

New processors

99x4 64 pin plastic package

⇒ multiple process incorporation
⇒ expanding address space (separate memory management)

MICROPROGRAMMED ARCHITECTURE
⇒ flexible instruction set.

9000 base set
⇒ base enhancement (signed multiply only)

9900 additions
⇒ byte string operations
⇒ shift operations
⇒ bit and period operations
⇒ multiplexed binary ops.
⇒ decrement operations
⇒ circular
⇒ floating point
Revisions in Antic.

All modes load the shift register on the first.

TWO PACKAGES.

BASIC BOX WITH CPU.

4K BITES RAM, TAPE

ANTIC

STELLA X

488 and/or RS232

GAME CONVERTER

I plug in RAM

SUGGEST FOR:

a) BASIC
b) SUPER GAMES
c) PHONE WORK
d) EDUCATION

PACKAGE

CONFIDENTIAL
ASIDE) ATARI SHOULD
START WITHIN 45
SMART TELEPHONE

Perhaps, delete T88
and define a special
bus—because
nothing needs the speed
except the disk.

Study CPU concept of
9902 same mode.

=) POKEY has P04
keys separate bus.
<table>
<thead>
<tr>
<th>Game or Project</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Minimum Box, LSI** - COINS $0.05-50$¢.

<table>
<thead>
<tr>
<th>CAU (6507, 6508, etc.)</th>
<th>MONITOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>6-8K bytes of ROM</td>
<td>CASE SET</td>
</tr>
<tr>
<td>4K bytes RAM,</td>
<td>CONTROL</td>
</tr>
<tr>
<td>PROGRAM, COMPLETION,</td>
<td>PANEL</td>
</tr>
<tr>
<td>SCREEN MAP.</td>
<td>SWITCHES</td>
</tr>
</tbody>
</table>

4

<table>
<thead>
<tr>
<th>P1(s) TYPE CONTROLLER</th>
<th>GAME CONTROLLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>PANEL SWITCHES.</td>
<td></td>
</tr>
</tbody>
</table>

6

<table>
<thead>
<tr>
<th>ANTIC</th>
<th>TV</th>
</tr>
</thead>
<tbody>
<tr>
<td>NON MOVING O.DEC.</td>
<td></td>
</tr>
</tbody>
</table>

4.5D

<table>
<thead>
<tr>
<th>TR-2</th>
<th>OBJECT GENERATION, ALLO</th>
</tr>
</thead>
<tbody>
<tr>
<td>POTY</td>
<td>KBD, POTS, SERIAL 20 KB EXPANSION.</td>
</tr>
<tr>
<td>LITE</td>
<td>R.B.</td>
</tr>
</tbody>
</table>

4.5D

<table>
<thead>
<tr>
<th>LSI.</th>
</tr>
</thead>
</table>

**Plays:**

<table>
<thead>
<tr>
<th>SIMULATED GAMES</th>
<th>(4 PINS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUNGEON SOFTWARE</td>
<td></td>
</tr>
<tr>
<td>SIMPLE BASIC</td>
<td></td>
</tr>
<tr>
<td>PROGRAM SOME GAMES.</td>
<td></td>
</tr>
<tr>
<td>COMPATIBLE WITH SIMULATED</td>
<td></td>
</tr>
</tbody>
</table>

**DOS CAS:**

<table>
<thead>
<tr>
<th>MURANO HOUSE</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>WILLIC (SPACE)</td>
<td></td>
</tr>
<tr>
<td>BURGULAR ALARM</td>
<td></td>
</tr>
<tr>
<td>2NO TYPE</td>
<td></td>
</tr>
</tbody>
</table>

**2ND BOX:**

**PLUGS INTO #1:**

**2W 8K BUS EXPANSION.**

**BIG POWER SUPPLY.**

160 L2 4K240F-FIFTEEN.

488 BUS.

**RESIDENT DOS ROM.**

**Software for Ports #1 and #2:**

8K BYTES OF ROM.
2nd BOX.

COSTS,

$32

8K RAM.

$10

4K RAM, DOS, BOOTSTRAP, ET.

$6

6848 + DRIVERS.

$48

DISK CONTROL.

 Disc.

+ TWO SCREW DISK DRIVE.

HARDCOPY - USE DARTSCREW

OR SOME OTHER METHOD

Perhaps buy. $40.

THE CURTAIN & PLATINUM RIBBON

ASSEMBLY FROM A SCUM

TYPEWRITER CARTS OR

FUROSE TYPE MACHINE

ADD SMALL SCANNER (IN A DOT

MATION) AND FASCIMILE

TRANSMISSION BECOMES POSSIBLE.
GAME OR PROJECT

Cassette System.

MARKETS: Game Player
Small Business
Technical Service Market

CONSIDER USING

82523 or 825123
32x8 Bipolar PROM

PROBLEMS ASSOCIATED WITH

Portability - Requires 4 Bits/Point
AND EXTRA DUT CYCLE OR
PARAUX RAM.

CONFIDENTIAL
THINGS TO DO ON RETURN:

1. PUT ANTIC ON CLAY
   MACHINE AND TRY
   OUT EX TV TD UNSAT.
   ASPECT RATIOS OF GRAPHICS,
   CHARACTERS, RESOLUTION ON
   20, AND 40 CMOS SECTIONS.
   EXAMINE EFFECTS OF COLORED
   40 CMOS (140sec & 45sec"
   GRAPHICS) - ON COLOR TV.

D.R. Marcacci
936-3473

MOVED TO
22ND
9AM.

MEETING OF 9TH JAP
FILLS ACECH
BROWN
JINCH.

ACCEPTED JOHN'S CONCEPT
OF SET FRAME: TAPE
ANTIC E/T/A
PIK & POLY
CPU
4-BIOS ROM
4K RAM

EXPANSION BTC 104 CARD SLOTS
PML 3084
EXPANDER BASIC
ETC.

SHALL COMPATIBILITY NOT REQUIRED

WRITER: BREWER
DATE
WITNESS
DATE

CONFIDENTIAL
JAN'S PROPOSAL

DAGGER

GAME OR PROJECT

COLLINS

BASECUT ACCEMT
BY BROWN, ACORN, EULL, WHICH
Steve wants to sell capability

BEWARE TO BUILD THINGS ON IF IT'S CHEAP -
KEEP TOTAL NUMBER OF DIFFERENT COMPONENTS DOWN.
DON'T NICKEL AND DIME THEM TO DEATH

DIFFERENCES:

1) ADD SECOND I/O EXPANSION
    AND SINGLE CARTRIDGE EXPANSION

2) 2ND UNIT IS SINGLE PACKAGE
    OR/DUAL FLOPPYS, RAM, ROM, AND
    48K TYPE I/O - RATHER THAN AN UNLOAD MOTHERBOARD
    EXPANSION BOX

OUTLINE OF PROPOSAL

1) MAINFRAME IS ENVIRONMENT MACHINE
    VIDEO GRAPHICS
    DATES
    PHONE
    HOUSE CONTROL
    MUSIC
    SIMPLE PROGRAMMING
    SMART TERMINAL
CONFIDENTIAL

Steve's Focus:
1. X = 35 - 38 years
2. Red and orange colors

Shelf to be used in the video installation.

Small, well-processed crunching business processes

Suggest:
- Consumer electronics, including
- Statistical analysis
- Local processing, larger computers

2) 2nd special case for

Pics: Senior Design
Discs, iron, electron healthcare protocols
PAC STELLA

Got PAC Color Working!!

Things that helped:

1) Turn PAC Color Oscillator to 4.433613 MHz.

2) Put RF Amplifier on Video Output.

3) Finer Tuning on TV.

4) Changing Polarity of FLP Feed Output for Phase Alternation.

5) Adjusting Delay Line and Delay Carefully.

Running with HSync =

\[ 278 \times \frac{5}{4} \times \frac{1}{4.433613 \text{ MHz}} \]

No Fail Effects Noticed on Tanks or PAC Missiles.
GAME OR PROJECT

ANTIC

AUGUST 15, 16, 17, 18. WORKED ON ANTIC IN BESS VALLEY.

MONDAY: INSTALLED RF AMPLIFIER
PUT 40 CHAR/LINE ON SCREEN.
IN BLACK AND WHITE, ON 4 GRAN
COM Tv (15"?)

RF VIDEO SUMMING,

RF INTERFERENCE ISOLATION,
AND RF AMPLIFICATIONS IS

BASICALLY IDENTICAL TO

STELLA, W/TWO EXCEPTIONS:

1) NO COLOR BURST,

2) RF AMP USED TO REDUCE NOISE FROM INTERFERENCE
FROM BREADBOARD AND PPP-11 CAPTAIN NEARBY.
GAME OR PROJECT

ANTIC BRIDGE BOARD

COMMENTS: AS CAN BE SEEN FROM
POLOPHOTO (SK-70) PHOTOS ON PREVIOUS PAGE,
CHARACTERS ARE SHARP IN BLACK AND WHITE.
DEPENDING ON UNIT/UNIT, SOMETIMES BLACK OR WHITE
LOOKED SHARPER THAN WHITE OR BLACK.

SMALLEST CHARACTERS ARE 40 (5X8) / LINE.
DOT CLOCK = 24 NTSC COLOR = 7.16 MHz.
(COLOR BURST NOT ON!)

TUESDAY 16 AUGUST

ADDED COLOR BY USING 14 MHz AND

SUB HARMONICS TO GENERATE
COLOR WITH A PROM. OTHER
INPUTS WERE USED TO SELECT
COLORS AND LUMINOSITY, AND
COLOR (20-80).

825129 20X4

<table>
<thead>
<tr>
<th>10k</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
</tr>
<tr>
<td>02</td>
</tr>
<tr>
<td>47</td>
</tr>
<tr>
<td>01</td>
</tr>
<tr>
<td>47</td>
</tr>
<tr>
<td>04</td>
</tr>
<tr>
<td>27k</td>
</tr>
<tr>
<td>15k</td>
</tr>
<tr>
<td>22pF</td>
</tr>
<tr>
<td>2.5k</td>
</tr>
<tr>
<td>14.32 MHz</td>
</tr>
</tbody>
</table>

WRITE: JES DUNN
DATE: 16-9-77
WITNESS: DUNN
DATE: 16-9-77
As can be seen in the first part,
courses work. In the horizontal
bands 1, 2, 3, 4. Screen map codes are
tested.

Band 1 is the 40 bit mode:
10 DMA's / line $\Rightarrow$ 5 x 8 x 2 = 80 x 2 bits
& 40 points, 4 color clocks x 8 lines
x 4 colors. (Stella PF resolution)

Band 2 is the 20 point mode:
20 DMA's / line $\Rightarrow$ 10 x 80 x 2 = 80 x 2 bits.
Each point 2 color clocks x 4 colors x 8 lines
(approximately partial resolution)

Band 3 is 3 repetitions of the 160 point mode:
40 DMA's / line $\Rightarrow$ 20 x 80 x 2 = 160 x 2 bits.
Each point 1 clock x 2 lines x 4 colors
(Stella QBERT resolution)

Band 4 same as Band 1.

At the top of screen, 20 and 40 character
lines are displayed with colors. Note that
the chroma carriers work with the luminance
with peculiar results. This begins
further study (What if color burst
was on, but no color carriers
during the line?)

Writer: Jose DeCuir
Date: 8/14/77
Witness: }


Sensitivity of Frequency

Code: Normal 4.4926417PS

Data Set: X = 0.13556, 0.492700 = 4.4926417PS
Niles' CKT PAL PAL COLOR.

3.546875 MHz PAL COLOR × 4)

(FAC LOW2) 4.53 MHz

27 PF

B2 PF

1 μF

1 μF

DSC DSC2

PAI TI1A

MASAR

PASS LOCKED

PAL COLOR 4.536 MHz 3
EXTENDED COIL 2

MODE

000
BLANK
1C (1-7 LINES)

001
20 CHAR/LINE
2 COLOR BITS X 8 BIT VIS.
2ND CHAR + 2 COLOR BITS,
8 LINES X 8 SECONDS.

010
40 CHAR/LINE
2ND CHAR + INVERTED.
10 LINES X 4 CHAR
< JUMP LINE

011
SPACE

100
SPACE

101
MENU MAP
40 BIT/LINE
X 8 LINE
3 DIA/LINE

110
MENU MAP
80 BIT/LINE
X 4 LINES
10 DIA/LINE

111
MENU MAP
160 BIT/LINE
X 2 LINES
70 DIA/LINE

CONFIDENTIAL
## Mode Summary To Date

<table>
<thead>
<tr>
<th>CODE ?</th>
<th>MODE</th>
<th>DESCRIPTION</th>
<th>ELEMENT SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLANK</td>
<td></td>
<td>15x158 LINES, BLANK</td>
<td>15x158 LINES</td>
</tr>
<tr>
<td>20 CHAR 1</td>
<td>8x8x1 CHAR x 2 COLOR 2 BITS</td>
<td>8 LINES x 8 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>20 CHAR 2</td>
<td></td>
<td></td>
<td>8 LINES x 8 CLOCKS</td>
</tr>
<tr>
<td>20 CHAR 3</td>
<td>8x8x2 CHARACTERS</td>
<td>8 LINES x 8 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>20 CHAR 4</td>
<td></td>
<td></td>
<td>8 LINES x 8 CLOCKS</td>
</tr>
<tr>
<td>40 CHAR</td>
<td>8x8x1 CHAR x 1 INVERT BIT</td>
<td>10 LINES x 8.5 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>40 CELL 1</td>
<td>4x2 (1 BIT SQUARES)</td>
<td>8 LINES x 4 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>40 CELL 2</td>
<td>4x2 (2 BIT SQUARES)</td>
<td>8 LINES x 4 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>80 CELL 1</td>
<td>1 BIT SQUARES</td>
<td>4 LINES x 2 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>80 CELL 2</td>
<td>2 BIT SQUARES</td>
<td>4 LINES x 2 CLOCKS</td>
<td></td>
</tr>
<tr>
<td>160 CELL 1</td>
<td>1 BIT SQUARES</td>
<td>2 LINES x 1 CLOCK</td>
<td></td>
</tr>
<tr>
<td>160 CELL 2</td>
<td>2 BIT SQUARES</td>
<td>2 LINES x 1 CLOCK</td>
<td></td>
</tr>
</tbody>
</table>

CLOCK = 3.55 ns
6 Color Lum Registors in TIAZ:

<table>
<thead>
<tr>
<th>AT2</th>
<th>AT1</th>
<th>HTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>φ</td>
<td>φ</td>
</tr>
<tr>
<td>1</td>
<td>φ</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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<td>φ</td>
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<tr>
<td>φ</td>
<td>φ</td>
<td>φ</td>
</tr>
<tr>
<td>φ</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- Column PP: P0, 20 char x 4 color
- Column P1: P1, 20 char x 4 color
- Column P2: P2, 20 char x 4 color, extended color
- Column P3: P3, 20 char x 4 color, extended color
- Column PF: RAW color, blank, extended color
- Column BK: Default - " ", blank mode
- Force white: 40 char mode
- Force blank:utar u blanking

3 Communication Lines Between ANTIC and TIAZ with Parallels Simultaneous Phase 3.58 MHz Clocks.
EXAMINING 1 BORROWED BASIC SPACE MACHINES.

38 KEYS.

40 INDICATOR LED ON MAIN.

40 INDICATOR LED ON TOP

MULTI-POSITION SYNTHETIC PAPER INTERFERENT

3 JACKS ON BACK FOR TAPE AND AC.

(INTERNAL OR APPEARANCE?)

ONE EXPANSION BUS CONNECTOR. (40PIN)

300 BAND TAPE FORMAT.

GRAPHICS ARE BLACK & WHITE

GRAPHERS 1 LEVEL, 10X10

OR 728X48X1 GRAPHICS.

IF THIS MONITOR THAT YOU ENTER

OF GAME KEY

NOW LOADED READY AND

WRITTEN IN BASIC. THIS

allows YOU TO TEST THE PROGRAM.

EXTERNAL TRANSFORMERS, INTERNAL TRANSFORMERS, INC.

12A 07 AC

WITNESS

DATE

8-3-80

8-3-80
CONFIDENTIAL

SIN-FUCK

BRIAN

BILLY BRUSH

BRYNN BERGER

DANNY DABLEY

JON ELLIS

LOOK AS SIN-FUCK'S LIST FIRST.

SINGLE FCT LINE -

HATT ACCESSOR AND

TRI STACK BUSES.

ASK FOR A SPECIFICATION

BEING 8 PIN, $1 IN, $1 OUT, $2 OUT.

P. C.V.I.N.B.

MAKE BREAK TO SEP NiCH

VECTOR - UNLOAD 2805R B1.

AND WORK CATCH

APE

PULL AUTO INCREASE.
JAY'S REQUEST FROM TADARO

4 C64 RAM
100$ CADDICODE CARTRIDGE $120$ CARTRIDGES
WIRE & RESISTOR KIT
VGA & SOUND EXCHANGE
8X1 CREATORS PROBE
100$ RESISTOR, CAPACITORS
(CRUM CARTRIDGE)
ANTIC & J3800 VIAs
2 CASSETTE JACKS
W/MOTOR START STOP
AUTOMATIC REELING
LITHE PEN
AUDIO AND DIGICOM ON THEIR

JAY SAYS 8589 IS
816 WORK, BECAUSE OF THAT.

WHAT IS SENSITIVITY OF SCHEDULE
US FEATURES

HOW FAST CAN WE BRING UP OTHER DEVICES
WHEN VS-1, VS-2, VS-3, VS-4?

PAGES CONTINUE
<table>
<thead>
<tr>
<th>C2</th>
<th>C1</th>
<th>C0</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C2</td>
<td>C1</td>
<td>C0</td>
<td>Color</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
<td>----</td>
<td>-------</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C2</td>
<td>C1</td>
<td>C0</td>
<td>Color</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
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</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Display List**

- MODE
- SCROLL
- BUS
- FIELD

**Control Code**

- LOAD T

**GAME OR PROJECT**

- C2 C1 C0
- Color
- Mode

**CONFIDENTIAL**

- BUCHNL
- 20CH3C1L
- 20CH3C2L
- 20CH4C1L
- 20CH4C2L
- 40CH
- 40D2C8L
- 40D4C8L
- 50D2C4L
- 80D4C4L
- 160D2C2L
- 160D4C2L
- 160D2C4L
- 160D4C4L

**WRITE**

- Date
- Witness
<table>
<thead>
<tr>
<th>Type of Cycle</th>
<th>Mode</th>
<th>Address Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blank N</td>
<td>0000</td>
<td></td>
</tr>
<tr>
<td>40 CH</td>
<td>0010</td>
<td>BG 5 4 3 2</td>
</tr>
<tr>
<td>20 CH 5 col</td>
<td>0100</td>
<td>BG 5 4 3 2</td>
</tr>
<tr>
<td>20 CH 4 col</td>
<td>0101</td>
<td>BG 5 4 3 2</td>
</tr>
<tr>
<td>20 CH 5 col</td>
<td>0110</td>
<td>BG 4 5 4 3</td>
</tr>
<tr>
<td>20 CH 4 col</td>
<td>0111</td>
<td>BG 4 5 4 3</td>
</tr>
<tr>
<td>40 cell 2 col</td>
<td>1000</td>
<td>T-LATCH</td>
</tr>
<tr>
<td>40 cell 4 col</td>
<td>1001</td>
<td></td>
</tr>
<tr>
<td>80 cell 2 col</td>
<td>1010</td>
<td></td>
</tr>
<tr>
<td>80 cell 4 col</td>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>160 cell 2 col</td>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>160 cell 4 col</td>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>160 cell 2 col</td>
<td>1110</td>
<td></td>
</tr>
<tr>
<td>160 cell 4 col</td>
<td>1111</td>
<td></td>
</tr>
<tr>
<td>Refresh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mode Fetch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DR32</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
GAME OR PROJECT
ANTIC, TIA OBJECT COLLISIONS:

TIA DEVICES
TIA VIDEO:
- T70
- T9
- T91
- T92
- T93
- TBD = BOARD UNRECOGNIZED

ANTIC VIDEO

ECODIS: APF CODE $1 4COLOR SCREEN APF 4COLOR SCREEN 4COLOR SCREEN
PROW: APF CODE 4 5COLOR CHAR OR 4COLOR CHAR
ANTIC: AP1 CODE 5 ""
VIDEO: AP2 CODE 6 "" 5COLOR CHAR, 4COLOR CHAR, OR 4COLOR 8

ANTIC VIDEO MODES ARE EXCLUSIVE—
so no collisions need be detected among them.
The board generator can be cleared with the
playfield. Since no collision of significance
expected between it and antic
generated objects:

20 COLLISIONS BETWEEN 4 TIA
DETECTOR AND 5 DIFFERENT
EXCLUSIVE DECODERS.

6 MUTUAL COLLISIONS AMONG
4 TIA MOVING OBJECTS.
GAME OR PROJECT
ANTIC-TIA COLLISIONS - cont.

26 COLLISIONS.

TP\phi
TP1
TP2
TP3

TP\phi 0000
TP1 00
TP2 0
TP3

6 COLLISION LATCHES APPEARANCE

INTERACTS WITH 4 APF COLLISIONS

LOOKS LIKE 32 BITS
8\times 4 BYTES
OR 16 PAIRS

16 PAIR CONFIGURATIONS.

TP\phi . TP1 . TP2 . TP3
TP\phi . TP\phi . TP1 . TP2 . TP3

OR
TP\phi . TP1 . TP2 . TP3
TP\phi . TP\phi . TP1 . TP2 . TP3

207,208

DATE
##_pins and addresses#

### 8 bit inputs

<table>
<thead>
<tr>
<th>Write Addresses</th>
<th>1-2-3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>COLCNF</td>
<td>1, 2, 3</td>
<td></td>
</tr>
<tr>
<td>GPLF</td>
<td>1, 2, 3</td>
<td></td>
</tr>
<tr>
<td>HPSF</td>
<td>1, 2, 3</td>
<td></td>
</tr>
<tr>
<td>MSDF</td>
<td>1, 2, 3</td>
<td></td>
</tr>
<tr>
<td>UDBFLP</td>
<td>1, 2, 3</td>
<td></td>
</tr>
</tbody>
</table>

**Total write addresses: 20**

### Read Addresses

<table>
<thead>
<tr>
<th>16 collisions</th>
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<tbody>
<tr>
<td>COLCNF</td>
</tr>
<tr>
<td>COLBK</td>
</tr>
<tr>
<td>CTRLF</td>
</tr>
<tr>
<td>CTRLBD</td>
</tr>
<tr>
<td>CYCLR</td>
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</tbody>
</table>

**Total read addresses: 25**

### PINS

<table>
<thead>
<tr>
<th>Pins</th>
<th>VSS, VCC</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK (3.5V)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Sync (MNTC)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PCE, q'2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>D4-D7</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>A0-A4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>A0/A1, 2</td>
<td>3</td>
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<tr>
<td>LEO1, 2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>CHADVD, D2</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

**Total pins: 28**

---

**Witness: Joseph Delora**

**Date: 25 Oct**
CONCEPT FOR PROTOTYPE SYSTEM
DISPLAY UNIT.

CONCEPT FOR PRODUCTIVITY SYSTEM
DISPLAY UNIT.

BUILD A WORKING CONCEPT UNIT.

CONNECT THE EXPANSION BUS.
ADD A BOX THAT ACCOMODATES LABORATORY
AND DEBUGGING OF APPLICATIONS
PROGRAMS. USE RESIDENT
KEYBOARD AND TV SCREEn FOR
COMMUNICATION WITH DEBBUGING MONITOR.
**GAME OR PROJECT**

**DATE**

**PINS**

<table>
<thead>
<tr>
<th>PIN</th>
<th>2</th>
<th>1</th>
<th>2</th>
<th>1</th>
<th>8</th>
<th>10</th>
<th>1</th>
<th>3</th>
<th>2</th>
<th>39</th>
<th>40</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC, VSS, CK</strong></td>
<td>VCC, VSS</td>
<td>3.5V Supply</td>
<td>CTC Mains</td>
<td>BUS Control</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td><strong>#1, #2</strong></td>
<td>TSC, PH-</td>
<td>Bus Control</td>
<td>BURST OUT CONTROL</td>
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<tr>
<td><strong>CS</strong></td>
<td>CDTC, GS1</td>
<td>BURST CHIP SELECT</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>DB4-DB7</strong></td>
<td>DATA BUS</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>GS4-GS15</strong></td>
<td>GND</td>
<td></td>
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<td></td>
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<tr>
<td><strong>SINC, 1</strong></td>
<td>SINC, 1</td>
<td>SINC, 1</td>
<td>VIDEO TO TV2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>AV1, AV2</strong></td>
<td>GND, AV1, 2</td>
<td>VIDEO TO TV2</td>
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</tr>
<tr>
<td><strong>CS4, CS10</strong></td>
<td>40 PIN, 400</td>
<td>COMPOSITE SYNC, 40 PB. LUM DATA</td>
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<tr>
<td><strong>PLS</strong></td>
<td>UP</td>
<td>LIGHT PYN ?</td>
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**PINSOUTS**

<table>
<thead>
<tr>
<th>PIN</th>
<th>2</th>
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<th>2</th>
<th>4</th>
<th>3</th>
<th>8</th>
<th>10</th>
<th>1</th>
<th>3</th>
<th>2</th>
<th>39</th>
<th>40</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC, VCC, GND</strong></td>
<td>0V</td>
<td>CLOCK</td>
<td>Horizontal from HSYNC</td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>#2</strong></td>
<td>SINC</td>
<td>HSYNC FROM HSYNC</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SINC</strong></td>
<td>PINT (D0)</td>
<td>PINT COMPONENT PROJECT</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td><strong>CS</strong></td>
<td>GND</td>
<td>CHIEF SELECT</td>
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</tr>
<tr>
<td><strong>AV1, AV2</strong></td>
<td>D4-D7</td>
<td>ADDRESSES IN</td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>D1-D7</strong></td>
<td>P1-0</td>
<td>DYN BUS</td>
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</tr>
<tr>
<td><strong>RI-0</strong></td>
<td>P4-P7</td>
<td>POT INPUTS</td>
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</tr>
<tr>
<td><strong>RI-P7</strong></td>
<td>D4-P7</td>
<td>POT ROLL-OFF</td>
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<tr>
<td><strong>P3-P12</strong></td>
<td>GND</td>
<td>BACK (OPAQUE SCAN OUTPUTS)</td>
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<tr>
<td><strong>AV1-0</strong></td>
<td>BOLD</td>
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<td></td>
</tr>
<tr>
<td><strong>AV1, 2</strong></td>
<td>BOLD</td>
<td></td>
<td></td>
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<td></td>
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</tr>
</tbody>
</table>

**WRITER**

Joe Dell Jr

**DATE**

**WITNESS**

**DATE**
2 Cells

\[ \Phi_1, \Phi_2 \text{ SPURIOUS } R_2 \text{ BUS } \text{ IN ARLENE} \]

3.5 MHz

[Diagram of circuitry]

**Output Shift Register Cell**

LOAD - DURING 1-7 SHIFT CYCLES

LATCH DATA - FROM FLIP-FLOPS

DBMSRFG

PICTURE STAGE

SAMPLE/HOLD

[Another diagram of circuitry]
CONVERSATION WITH...

ANTIC PINS...

DON'T PUT LIGHT PINS IN.

DON'T CONNECT EXTRA SYNC TO THIS.

US C57 PLUG.

ARE SYNC CONNECTORS NEEDED HERE?

1 ANTIC HAS 20 PINS.

2 PINS FOR DMA GIANT, DMA REQUEST.

SIEVE SUGGESTS SCROLLING

WHOLE SCROLL BY SHIFTING.

SYNC TO BLANK.

LEAVE OUT SIEVE SCROLL.
GAME OR PROJECT

**RAYZ**

WIRE DO KEYBOARD WITH TWO MAX232s. 4051 B DUE.

47K

G4

SCANNED 52, 47K.

- 64 SCANNED KEYS

\[ \frac{5}{5+47} = \frac{5}{52} \times 5.01 \]

4051

< 2.5K

- 7K
KEY BOARD MUST BE SEXY!

FANCY GAME PLAYER THAT
YOU CAN PLAY IT IN BASIC
JAH BUS accepts 8PINS (cf. routing shows)
FULL UPDATE INTO CASSETTE.

4 CONTROLLER CONNECTORS.
G.PIN.
SAME AS STARRA.

STANDARD PADD.

2x12, 82 G.PIN.
50-50 G.PIN
SMB BUS
BINARY ROMS.

RF CASE.
GAME OR PROJECT: ANTIC, TIA.

For automatic object generation:
Take refresh cycles.
Have TIA recognize them.
Add base pointer to refresh.

Base Reg.    | B Refresh
-------------|-----------
1 1 1 1 1    | V7 V6 V5 V4 V3 V2 V1 V0 H1 H2

For fetching object graphics out of memory:
TIA can accept those graphics.

Base Reg
AHA:

Bus Addresses

BAD  V0 H3 H2 V7 V6 V5 V4 V3 V2 V1

RAM CHIP
PROJECT GENERATION

DIFFERENT REFRESH CYCLES FROM

OBJECT FETCH CYCLES.

AB 15  CBL 15
  14  CBL 14
  13  CBL 13
  12  CBL 12
  11  CBL 11
  10  CBL 10
   9  H3 or D3 L9
   8  H2 or H3
   7  DBC 7 or H2
   6  DBC 6
   5  DBC 5
   4  DBC 4
   3  DBC 3
   2  DBC 2
   1  DBC 1
   0  DBC 0

0 0 0 0

TL 15 TL 14 TL 13 TL 12 TC 11 TC 10

DLC 9 DLC 8 DLC 7 DLC 6 DLC 5 DLC 4 DLC 3 DLC 2 DLC 1 DLC 0

TC 9  TC 8

TC 7 TC 6

TC 5 TC 4

TC 3 TC 2

TC 1 TC 0
**Vertical 3 Delay**

In 128 Byte Table

<table>
<thead>
<tr>
<th>Line</th>
<th>(2^N)</th>
<th>(2^N+1)</th>
<th>(2^N+2)</th>
<th>(2^N+3)</th>
<th>(2^N+4)</th>
<th>(2^N+5)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>P1(N)</td>
<td>P1(N)</td>
<td>P2(N)</td>
<td>P3(N)</td>
<td>P4(N)</td>
<td>P5(N)</td>
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<tr>
<td>2</td>
<td>P1(N+1)</td>
<td>P1(N+1)</td>
<td>P2(N+1)</td>
<td>P3(N+1)</td>
<td>P4(N+1)</td>
<td>P5(N+1)</td>
</tr>
<tr>
<td>3</td>
<td>P1(N+2)</td>
<td>P1(N+2)</td>
<td>P2(N+2)</td>
<td>P3(N+2)</td>
<td>P4(N+2)</td>
<td>P5(N+2)</td>
</tr>
<tr>
<td>4</td>
<td>P1(N+3)</td>
<td>P1(N+3)</td>
<td>P2(N+3)</td>
<td>P3(N+3)</td>
<td>P4(N+3)</td>
<td>P5(N+3)</td>
</tr>
</tbody>
</table>

If not delayed, capture on 1st line.
If delayed, capture on 2nd line.

**REGISTERS IN ANTIC FROM CPU POINT OF VIEW**

<table>
<thead>
<tr>
<th>REG</th>
<th>Value</th>
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<tbody>
<tr>
<td>BC</td>
<td>X</td>
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<tr>
<td>OB3</td>
<td>X</td>
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<tr>
<td>TCON</td>
<td>Low</td>
</tr>
<tr>
<td>TLAH, TCH</td>
<td>High</td>
</tr>
<tr>
<td>R/W</td>
<td>??</td>
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<tr>
<td>ADDR</td>
<td>VCOUNT</td>
</tr>
<tr>
<td>READ</td>
<td>STATUS</td>
</tr>
<tr>
<td>WRITE</td>
<td>CTRL, TCON</td>
</tr>
<tr>
<td>WRITE</td>
<td>DCH1</td>
</tr>
<tr>
<td>WRITE</td>
<td>DCH2</td>
</tr>
</tbody>
</table>

Base Address Channels, base address objects, Memory Pointer "T".

3RD URBIC, CONTROL, INTERRUPT BIT, ETC.

Scrolling Offset Mode (DMA)
ANOTHER HOT IDEA.

GIVE TWO 8 BIT TIMED OBJECTS TO GET TWO MORE AND 4-COLOR POINT OBJECT

3.58

EACH OBJECT CAN BE INDEPENDENT (ONE LEVEL)
OR PAIRED (TWO LEVEL)

WRITER: D. C. U. R.  DATE: 10/27  WITNESS: Jay Miner  DATE:
GAME OR PROJECT

CAIERS: PASSARE (MINISTER)

29 NOV 77

JOE WANTS TO
DEFINE THE PRODUCT
AND GET IT OUT.

Two cartridges.

- Screws from W2. $2 $8
- 650-2 5.0
- RAM 4K 12.2
- RAM 4K 3.00
- ULA 3.0
- ATRIC 6.00
- TIM 7.50
- PAPYR 4.00
- NCE 7.50

TOTAL PARTS $115.17
LABOR 12

Cost to build $171.47 = $300!!

PROPOSED SOLUTIONS

"STUCK WITH THIS.

TWO PROPOSED PRODUCTS
GAME PLATINUM, NON-EXPANDABLE - $100 PER PARTS

"CANDY" PARTS $85.50 NO KEYBOARD
+ 9 $19.50 NO DISC DRIVE
AND CONTROLLER, CAPABIL. SAME IC

BAQT STILL NOT FCC APPROVED

DESIGN BUT MAY NOT INTRODuce
COLOR + BUILT IN COLOR MONITOR

"ELIZABETH" $100 13" COLOR MONITOR

PARTS $211 + 12 = $250
They expect to build skills into 3779.

Joe sees the test.

FC problem w/ Candy
UL problem w/ Elizabeth.

If chip set available in Nov 78
we can show in January.

John (unreadable) suggests
that Japanese may put
video input on future TVs.

Lots of chatter.

Perhaps add sexual xbow to Candy
delete Candy
build Elizabeth.
SYNTHIC / HUMBY

PRESENTATION

JACK BOURDO
ENGINEER PLACES
WITH ASSISTANT

MEMORIES, PERIPHERALS & MICROPS.

DID NOT GET 1000 DYNAMIC RAMS

(USING PHYSICIAN RESISTORS
IN PLACE OF 8 DEPARTMENT LOADS)

LIGNON WAS IT, TOO

WORKING ON 4-MARS.

16K STATIC II
4K X 4, OR 24 X 8
200 NSEC 15" SLOW"

DICK SAYS $3 00 2117 IN 1979
70MCG. 350 SEC.

WORKING FOR 4K X 15

S6509 - COMPUTRAH 1 X 2 52 USC.
GAME OR PROJECT
PACMAN - SYSTECH MEETING CONTINUES

6551 - AICA
6569
CRT CONTROLLER
FLOPPY DISK CONTROLLER

DO NOT ADAPT ON 6600 !!!

1600?

MOS NEW INSTRUCTIONS

RECOMMEND
6502 + 6530

COMPARABLE TO 3870

OUR DISCUSSIONS

DESIGN FOR M6512
PUSH DEVELOPMENT OF S6519/09
MAKE DECISION LATER TO USE 65/5012.
GAME OR PROJECT
PACMAN, SYNERGIC

6502  M6502  S6509

SOFTWARE COMPATIBLE  UPGRADE SOURCE COMPATIBLE
BC.  TILT.

TACT Compatible.

考试 [NOT NEEDED TO BE PINAT.

1ST PARTS ON M6502 END
1ST QUARTER.

QUESTIONS ASKED AND PARTIALLY ANSWERED

Q: WHAT IS REVEL JIN CAN?
   FOR 10?

ANS:
   COMPATIBLE W/SPECIFIED IF IT
   DOESN'T COST EXTRA.

   OPTIONAL KEYBOARD AND/OR
   AND CASSETTE-ROMACCESS
   THEN CONTINUE AS US.
   INTERFACE PARALLEL TO VIA.

   SD ANY SE
## Game or Project
**Candy** "Usi" Parts

### Pinouts & Interconnect

<table>
<thead>
<tr>
<th>Signal</th>
<th>G509 (P2)</th>
<th>ANTIC</th>
<th>CTIA</th>
<th>PIA-3</th>
<th>PIA-5</th>
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<tbody>
<tr>
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<td>Ucc</td>
<td>B</td>
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<td>Pots</td>
<td>Pots</td>
<td>40</td>
<td>Pots</td>
<td>40</td>
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</tr>
</tbody>
</table>

### Notes
- Writer: [Name]
- Date: [Date]
- Witness: [Name]
- Date: [Date]
Mike Albauch has convinced Jay to
lunch that the display list control should
A) be jam loadable.
B) jam load register load 0 87 CPU.
C) jam loadable 87 ah 8a code in
the display list (jump)
From two discussions on vertical scrolling:

Conclusions first:

CPM can now load a Delta register

Delta register or made PLA loaded into Delta counter.

Two stages locations:
- Start scroll:
  \( \Delta CR = \Delta REX \text{ instead of } \text{ mode PLA} \)
- End scroll:
  Mode fetch request set at \( \Delta REX = \Delta CR \)
  instead of \( \Delta CR = \Phi \)

Need from antic set at same time as mode fetch request (1 line ahead or mode fetch)

---

Horizontal scrolling:

Sup counter that is slide under once/line — scrolls to 1 complete clock resolution — used to generate T counter and graphics PLA fetches.

By computer clock (1 clock cycle) scrolling done with single 2nd request at output of most graphics PLA — just before antic output

\[ \text{Diagram} \]

Writer: Joe DeCuir  Date: 12/8/77  Witness:  

Date:
<table>
<thead>
<tr>
<th>Game or Project</th>
<th>Antic</th>
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**Inventory & Revisions:**

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<tr>
<th>NMI REQ</th>
<th>VD</th>
<th>0</th>
<th>0</th>
<th>Read</th>
<th>Write</th>
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<tr>
<td>NMI MASKS</td>
<td>VD</td>
<td>0</td>
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<td>Write</td>
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<td>NMI ACK</td>
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<tr>
<td>LP STATE</td>
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<td>ASCROLL Size, REC, CTRL</td>
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<td>DISPLAY LIST COUNTER</td>
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<tr>
<td>RESET HSYNC</td>
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<td>OBJECT SCAN ENABLE</td>
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<td>Write</td>
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</tbody>
</table>

**Notes:**

- Dutch
- ROM only
- Data only
- INVB
- Write
- Write 3 for testing
- Write
INVENTORY OF MODE CODES. (FROM PAGE 85)

0200 - 020F: BLANK (BACKGROUND) (3BIT N) (1-7) CPR
0210: JUMP (LINE BACKGROUND) AND PRINT 
0211: (70CH UPPER CASE)
0212: 40 CH UPPER AND LOWER CASE
0100 - 010F: 20 CH X 5 COLOR x 8 LINES
0101 - 010F: 20 CH X 5 COLOR x 8-2 LINES
0110 - 011F: 20 CH X 4 COLOR x 8 LINES
0111 - 011F: 20 CH X 4 COLOR x 8-2 LINES
(10 CELL X 2 COLOR X 8 LINES) DELETED
1100 - 110F: 40 CELL X 4 COLOR X 8 LINES
1101 - 110F: 80 CELL X 2 COLOR X 4 LINES
1110 - 111F: 80 CELL X 2 COLOR X 4 LINES
1111 - 111F: 160 CELL X 2 COLOR X 2 LINES
1110 - 111F: 160 CELL X 4 COLOR X 9 LINES
1111 - 111F: 320 CELL X 2 LEVEL X 1 LINE

CHARACTER ADDRESS FORMATS:

DATA ADDRESS: 86 5 3 2 1 5 3 1 2 11021

CHARACTER BYTE: 1 ADDRESS
COAST OF CHARACTER

DATA ADDRESS: 86 5 4 3 2 1 5 3 2 1 10121

CHARACTER BYTE: ADDRESS -> 2ND 2 COAST COLOR SELECT

WRITER: DECOR
DATE: 13.5.77
WITNESS
DATE
INTERRUPT STRUCTURE

RESET — ONLY POWER ON
AND ENDED BY BREAK KEY.

NMI — VIDEO INTERRUPTS
1. U BLANK
2. DISPLAY BLOCKS END

IRQ — NON U BLANK
1. KEYBOARD
2. SERIAL PORT
3. AUDIO TUNER
4. EXTERNAL DEVICES

U BLANK I/O DO NOT INTERRUPT DRIVERY.
MUGGER POTS NOT INTERRUPT DRIVERY.
JOYSTICKS NOT INTERRUPT DRIVERY.
POTS NOT INTERRUPT DRIVERY.

ANTIC
THAT POSSIBLY DNA.

JAY'S SUGGESTION — 14 DEC 77

BRING IN EXTERNAL EXPANSION
INTERRUPT VIA ONE OF C/A1, C/A2, P/B.

CONFIDENTIAL
GAME OR PROJECT

- DIGGY SERIAL PORT DISCUSSION w/MIKE

110, 300
1200, 2400, 4800
9600, 19200

MIKE SUGGEST 16x CLOCK

DOES NOT JUST TALK TO OTHER ATARI PRODUCTS.

MIKE RAISES ISSUES ABOUT

CLOCK TOLERANCE - SWEEING IF BUFFERS ARE NOT DEGENERATIVE - SYNCHRONOUS WITH CLOCK.

NEVER HAVE MORE THAN ONE BAND RATE OUT THERE AT ANY ONE TIME.

Perhaps the clock should be bidirectional.
Scott's suggestion:

In 20 Channel X 4 color,

Shift channel up

Instead of

<table>
<thead>
<tr>
<th>BC</th>
<th>13 2 1 0</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>LEFT/RIGHT DIP</td>
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Address

Shift convert up.

<table>
<thead>
<tr>
<th>BC</th>
<th>9 0 2 1 2</th>
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<tbody>
<tr>
<td></td>
<td>LEFT/RIGHT</td>
</tr>
</tbody>
</table>

2nd channel select.

How to do it.

Example, RAS 2.3

MAB 7

RAS 3

MAB 5

RAS 4
SUGGESTED ADDRESS DECODING SCHEME

- 4k0 - RESIDENT RAM, 000 - 100H
- 4k1 - EXPANSION RAM
- 4k2
- 4k3
- 4k4
- 4k5
- 4k6 - RESERVED FOR I/O
- 4k7 - RESIDENT RAM

CONFIDENTIAL
CONFIDENTIAL

6 DATA SEQUENCES:

1. 40 CELL/4 COLOR, 50 CELL/2 COLOR
   10 DMA/LINE 1ST LINE ONLY

2. 50 CELL/4 COLOR, 160 CELL/2 COLOR
   20 DMA/LINE 1ST LINE ONLY

3. 160 CELL/4 COLOR
   40 DMA/LINE 1ST LINE ONLY

4. 20 CHARACTER/5 COLOR
   20 + 20 DMA 1ST LINE
   20 DMA/LINE THEREAFTER

5. 20 CHARACTER/4 COLOR
   20 + 40 DMA 1ST LINE
   40 DMA/LINE THEREAFTER

6. 40 CHARACTER/2 COLOR
   40 DMA 1ST LINE
   40 DMA/LINE THEREAFTER

LEADS BY 4 CICLUS
4 CICLUS TOTAL
2 CICLUS FREE

LEADS BY 4 CICLUS
4 CICLUS TOTAL
2 CICLUS FREE

LEADS BY 4 CICLUS
6 CICLUS TOTAL
4 CICLUS FREE

LEADS BY 4 CICLUS
8 CICLUS TOTAL
4 CICLUS FREE

LEADS BY 4 CICLUS
6 CICLUS TOTAL
2 CICLUS FREE

WRITER: DeCure
DATE: 6/3
WITNESS
DATE
GAME OR PROJECT
ANTS CHIP DMA TIMING

T LEADS BY 4 CYCLES.

(from JAYS Timing Diagrams)

MEMORY MAP DMA SEQUENCES
40, 80, 160, 400

CYCLE LENGTH
TO FIRST BIT

DISPLAY BOUNDARY

70 CHAN/SCROLL
DESIGN of
Man Computer Dialogues

James Martin
C51-8

Practice Hall
1750

Englewood Cliffs, N.J.

RICK MUNCRIFIC

MORGAN HOFF

Team #4 2642

CONFIDENTIAL